



# Technical Document

## Yosys

Version 0.0.1

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# 1 Software installation

## 1. Visit homepage and download the setup file

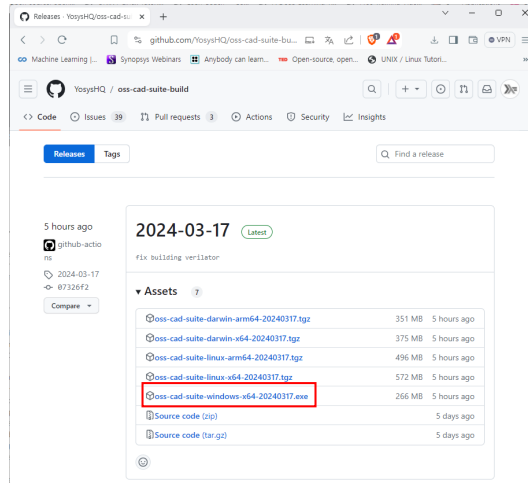


Figure 1: Visit homepage and download setup file

## 2. Click “추가 정보”

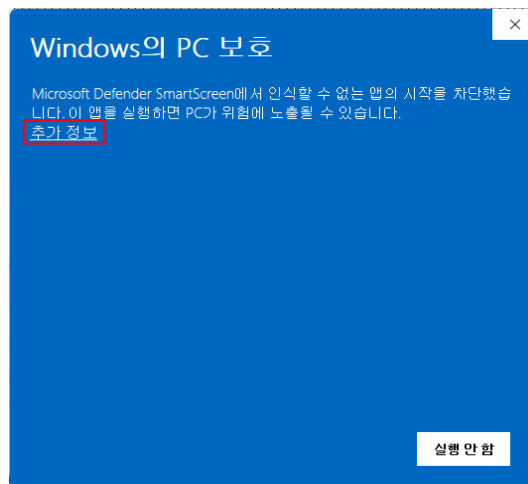


Figure 2: Click 추가 정보

### 3. Click “실행”

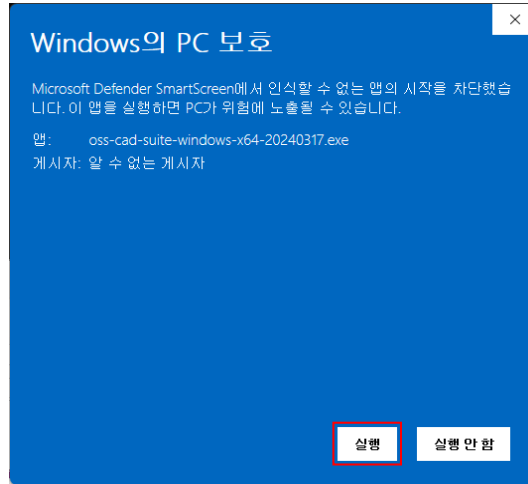


Figure 3: Click “실행”

### 4. Upon installation complete, “oss-cad-suite” folder is created

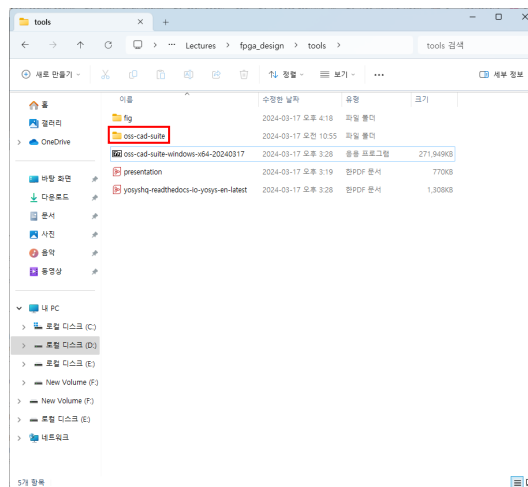
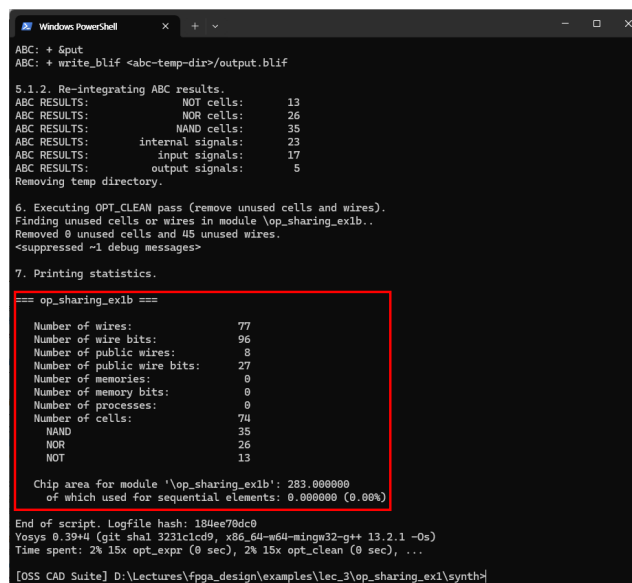


Figure 4: Installation complete

## 2 Examples

1. Download the example from [link](#)
2. Decompress the downloaded “op\_sharing\_ex1.zip”
3. Open “Windows PowerShell”
4. Browse the “op\_sharing\_ex1\synth” folder
5. Execute the following commands
  - path\_to\_oss\_cad\_suite\environment.bat
  - path\_to\_oss\_cad\_suite\start.bat
6. Type “yosys synth.y” to view to synthesis result



```
Windows PowerShell
ABC: + $put
ABC: + write_blif <abc-temp-dir>/output.blif

5.1.2. Re-integrating ABC results.
ABC RESULTS:      NOT cells:      13
ABC RESULTS:      NOR cells:      26
ABC RESULTS:      NAND cells:     35
ABC RESULTS:      internal signals: 23
ABC RESULTS:      input signals:   17
ABC RESULTS:      output signals:   5
Removing temp directory.

6. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \op_sharing_ex1b..
Removed 0 unused cells and 445 unused wires.
<suppressed -1 debug messages>

7. Printing statistics.

=== op_sharing_ex1b ===
Number of wires:          77
Number of wire bits:     96
Number of public wires:   8
Number of public wire bits: 27
Number of memories:      0
Number of memory bits:   0
Number of processes:     0
Number of cells:         74
NAND                     35
NOR                       26
NOT                       13

Chip area for module '\op_sharing_ex1b': 283.000000
of which used for sequential elements: 0.000000 (0.00%)

End of script. Logfile hash: 188ee78dc0
Yosys 0.3944 (git sha1 3231c1cd9, x86_64-m64-mingw32-g++ 13.2.1-0s)
Time spent: 2% 15x opt_expr (0 sec), 2% 15x opt_clean (0 sec), ...

[OSS CAD Suite] D:\Lectures\fpga_design\examples\lec_3\op_sharing_ex1\synth\
```

Figure 5: Synthesis result