Create Project in Vivado

1. Create Project
2. Project name & location
3. Select "RTL Project – Do not specify sources at this time"
4. Boards – Vendor: Xilinx – Name: Spartan-7 SP701 Evaluation Platform
5. Finish

Add RTL Design

1. Add Sources
2. Select "Add or create design sources"
3. Create File
4. File type & name
5. Specify input and output ports (optional)
6. Sources – Design Sources – Verilog file

```
module LED(
    input SW,
    output LED
);
    assign LED = SW;
endmodule
```

Simulation

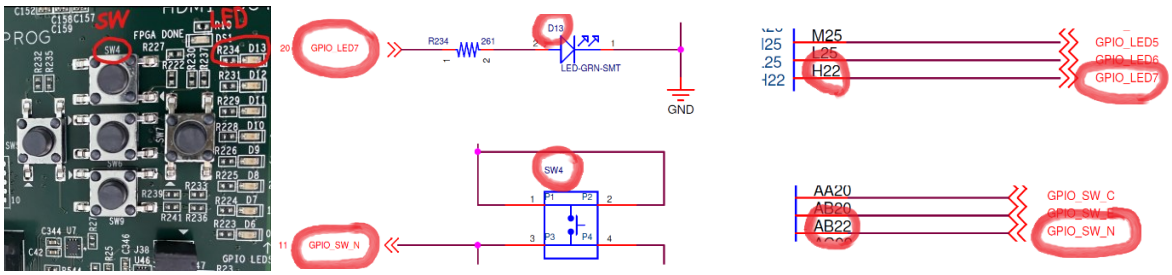
1. Add Sources
2. Select "Add or create simulation sources"
3. Create File
4. File type & name
5. No input & output specification
6. Sources – Simulation Sources – sim_1 – Verilog file

```
module LED_TB();
    reg SW;
    wire LED;
    LED uut(
        .SW(SW),
        .LED(LED)
    );
    initial begin
        SW = 1'b0;
        #100 SW = 1'b1;
        #200 SW = 1'b0;
        #100 SW = 1'b1;
        #100 SW = 1'b0;
    end
endmodule
```

7. Run Simulation – Run Behavioral Simulation

I/O Ports

1. RTL Analysis – Open Elaborated Design
2. Elaborated Design – I/O Planning
    A. SW: SW4, LED: D13 on SP701 board
    B. Open schematic, find SW4 and D13
    C. Find the pin that connects SW4 and D13 with the FPGA chip
    D. SW – SW4 – **AB22**, LED – D13 – **H22**
    (or refer to the XDC file)



3. I/O Ports – Scalar ports
    A. OUT – H22 – LVCMOS33 (I/O Std)
    B. IN – AB22 – LVCMOS33 (I/O Std)

4. Save Constraints

Synthesis

1. Run Synthesis
2. View Reports

Implementation

1. Run Implementation
2. View Reports

Program & Debug

1. Generate Bitstream
2. Open Hardware Manager
3. Open Target – Open New Target – Local Server – Select Xilinx board
4. Program Device – Program
5. Check FPGA_DONE LED (if it is blue, FPGA programing is done)
6. Debug