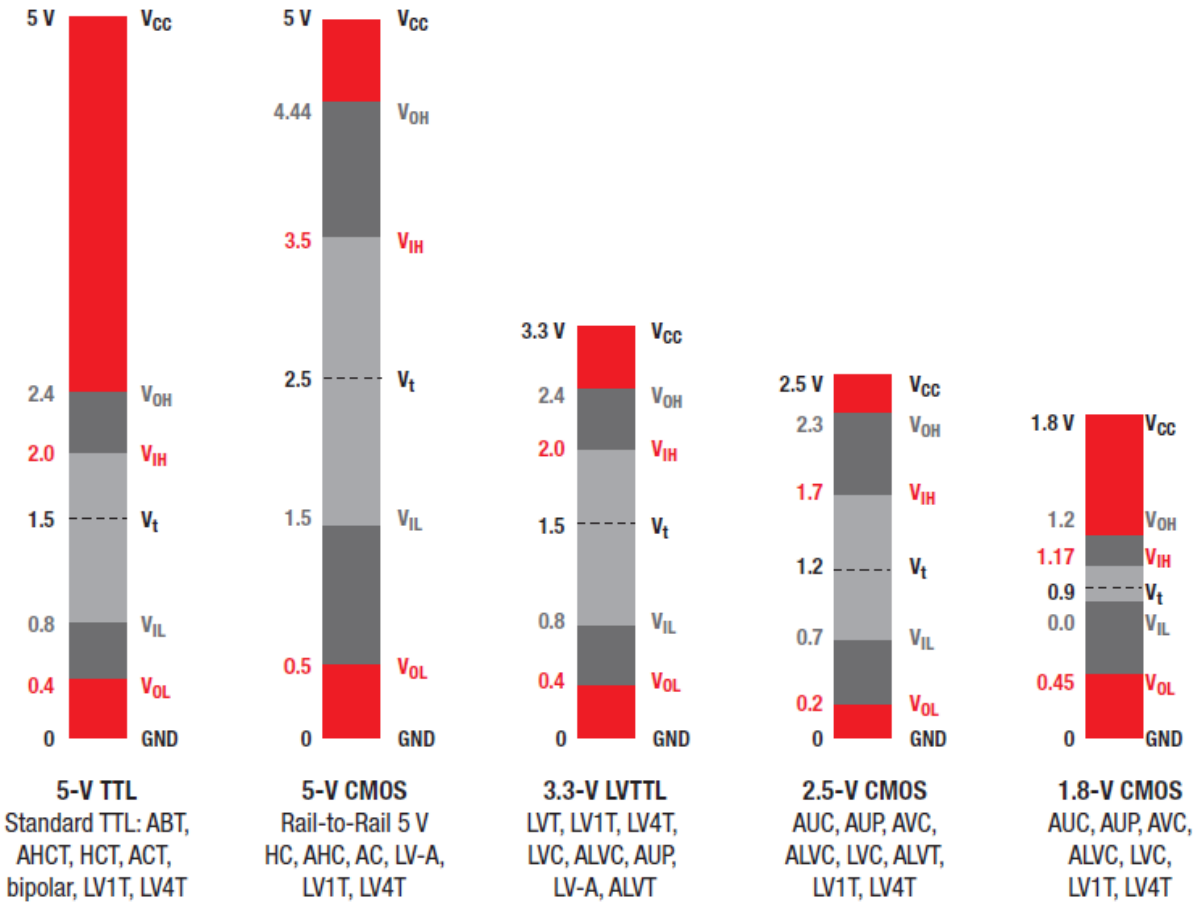
Lecture 03

논리 게이트

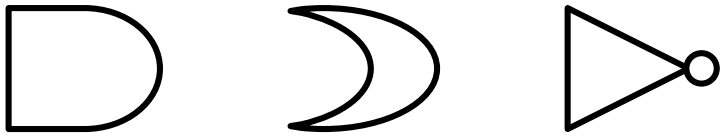
논리 레벨



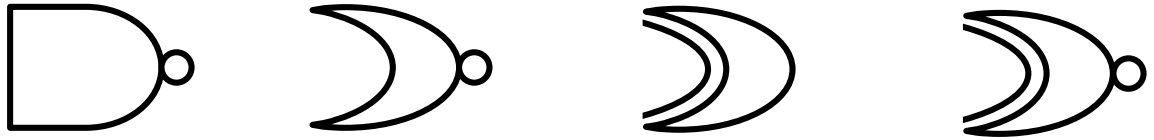
Source: Texas Instruments, *Logic Guide*, https://www.ti.com/lit/pdf/sdyu001 (accessed on 2024.08.05).

논리 게이트

- 기본 논리 게이트



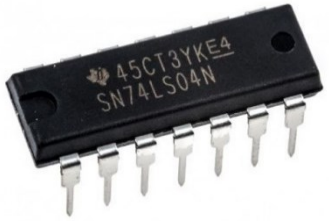
- 기본 논리 게이트의 조합으로 만든 게이트

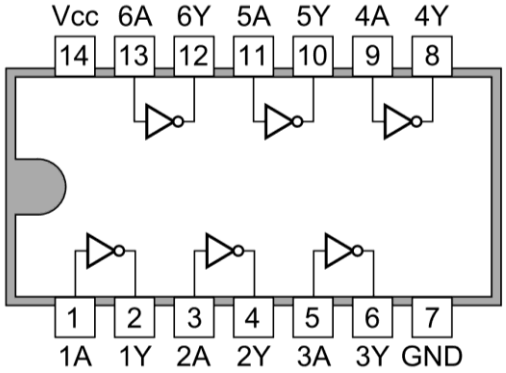


- 논리 게이트 → 조합논리회로 및 순서논리회로 → 디지털 시스템 → 컴퓨터 시스템

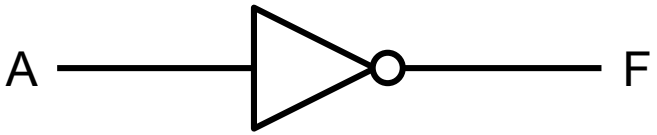
NOT 게이트

- 2진수의 논리 반전
  - 입력 한 개
  - 출력 한 개
  - $F = \overline{A}$
- 인버터(**inverter**)라고도 함





IC 7404 Inverters



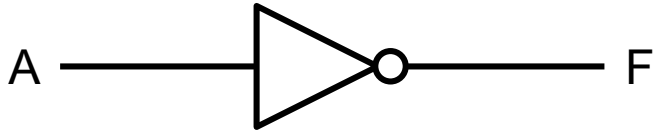
진리표(truth table)

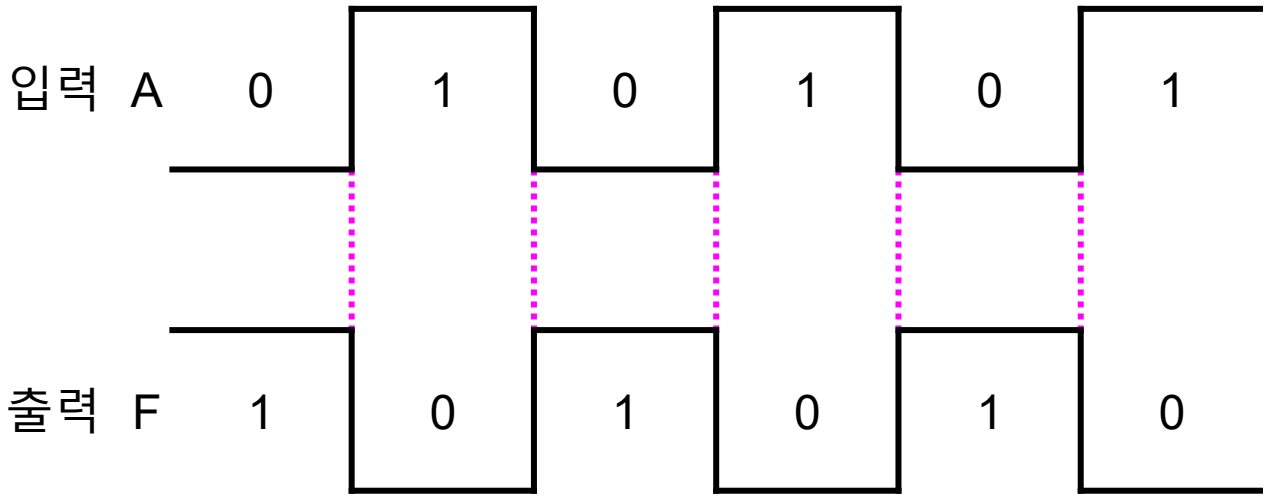
입력	출력
A	F
0	1
1	0

Source: STMicroelectronics, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/23020/ (accessed on 2024.08.05).

NOT 게이트

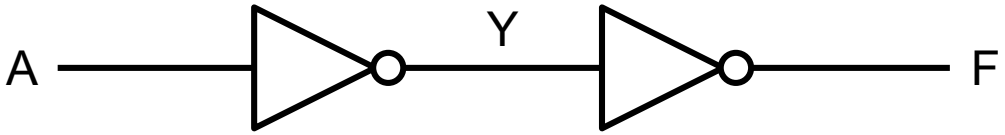
- 동작 파형

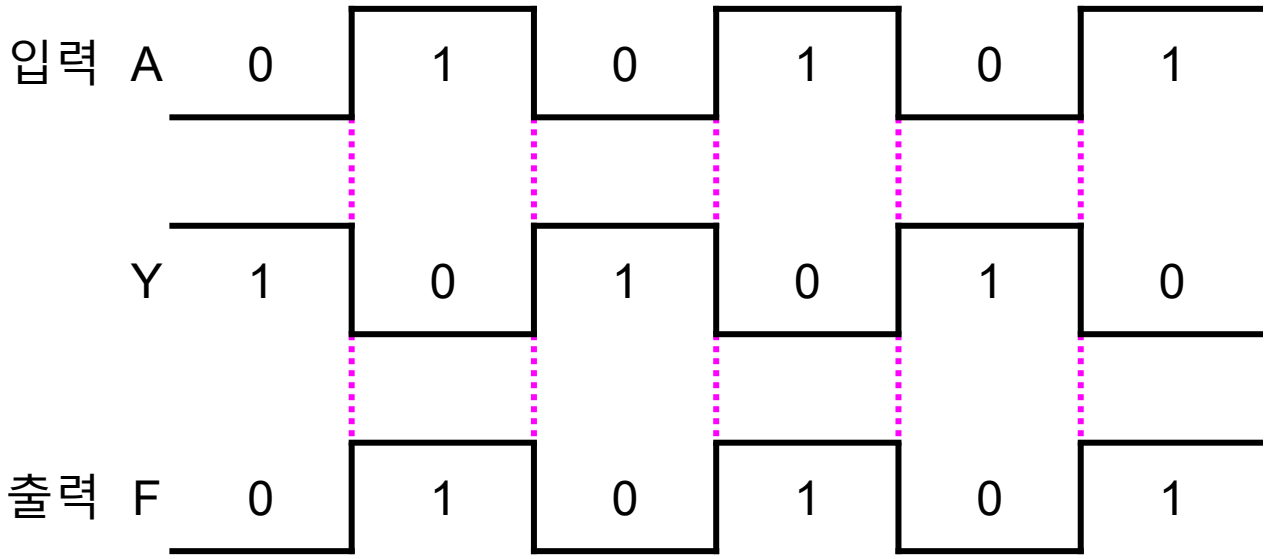




NOT 게이트

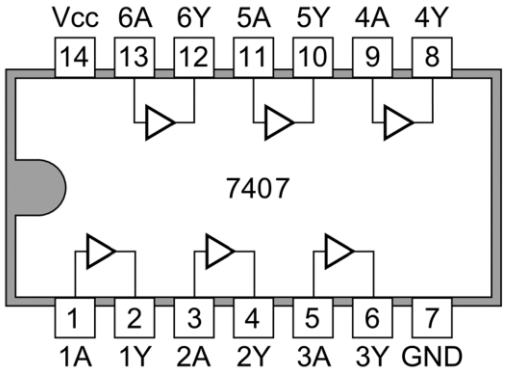
- 예,



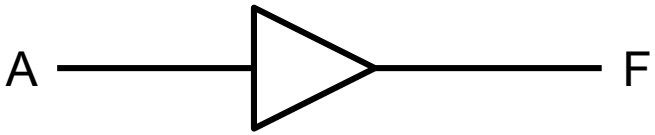


버퍼 게이트

- 입력된 신호 그래도 출력하는 게이트
  - 입력 한 개
  - 출력 한 개
  - F = A



IC 7407 Buffers



진리표

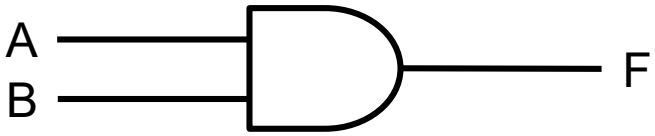
입력	출력
A	F
0	0
1	1

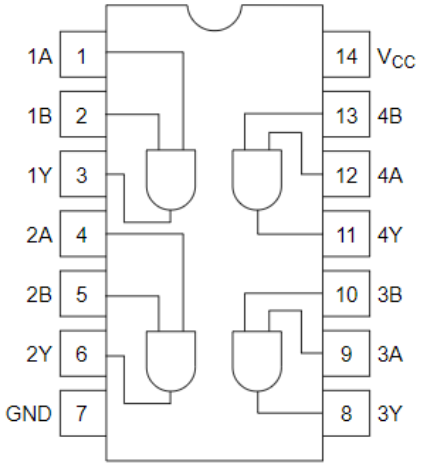
Source: Fairchild Semiconductor, *Datasheet*, https://pdf1.alldatasheet.co.kr/datasheet-pdf/view/50893/ (accessed on 2024.08.05).

AND 게이트

- 입력 **모두 1**인 경우에만 출력 **1** 됨
  - 입력 두 개 이상
  - 출력 한 개
  - 예, 2입력 AND 게이트의 경우 F = A•B = AB

2입력 AND





IC 7408 Quad 2-Input AND Gates

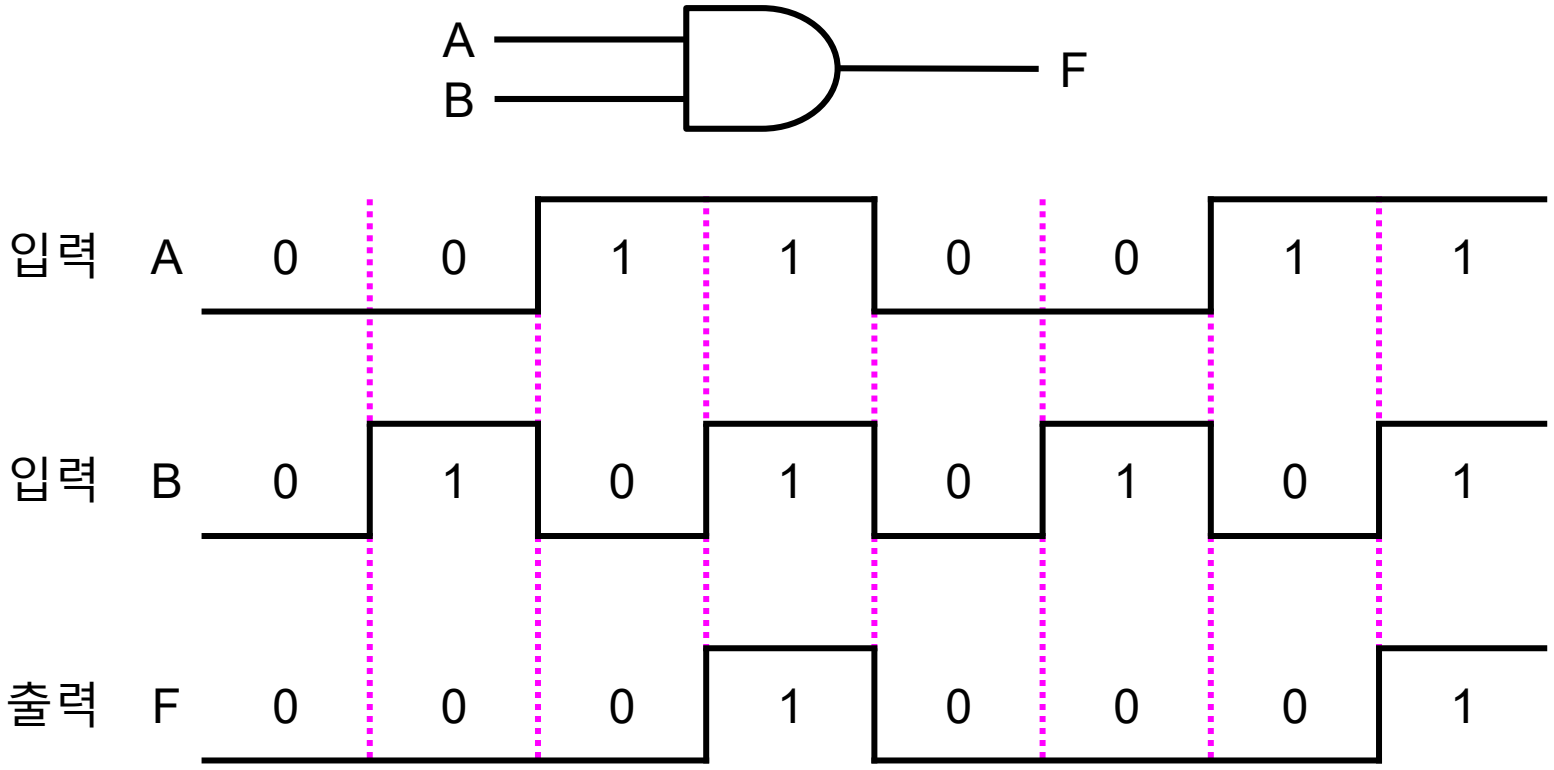
진리표

입력		출력
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Source: Hitachi Semiconductor, *Datasheet*, https://pdf1.alldatasheet.co.kr/datasheet-pdf/view/63807/ (accessed on 2024.08.05).

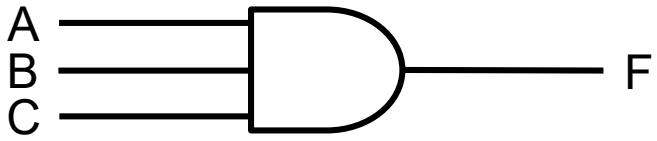
AND 게이트

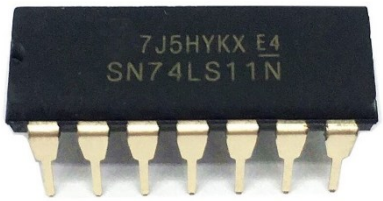
- 동작 파형

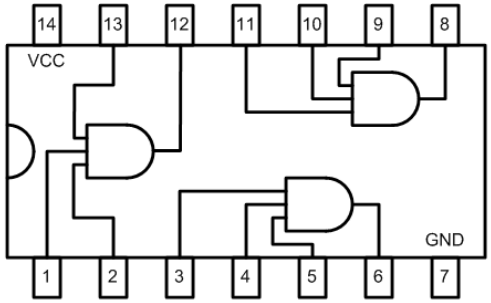


AND 게이트

- 3입력 AND 게이트
  - F = A•B•C = ABC







IC 7411 Triple 3-Input AND Gates

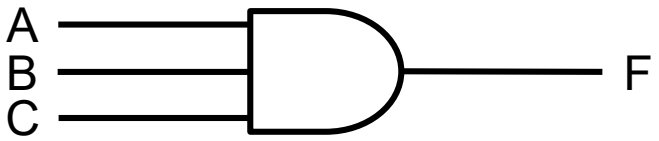
진리표

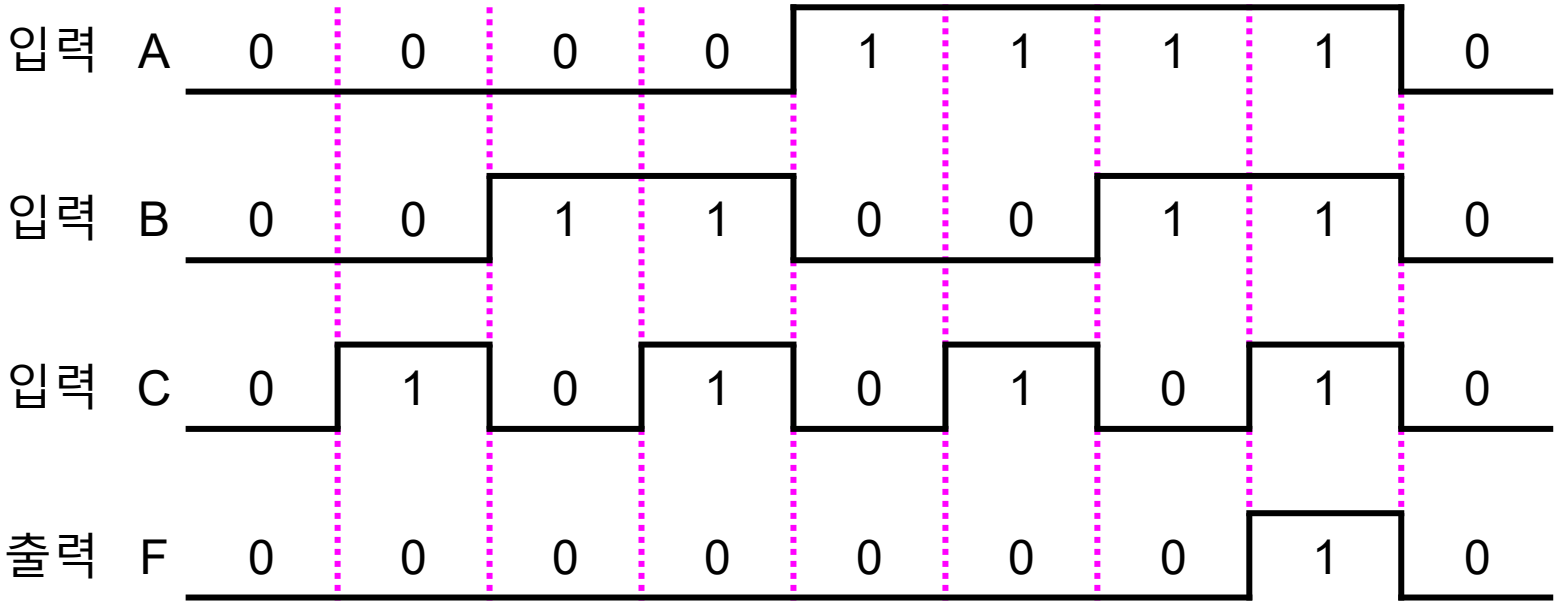
입력			출력
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Source: *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/125557/ (accessed on 2024.08.05).

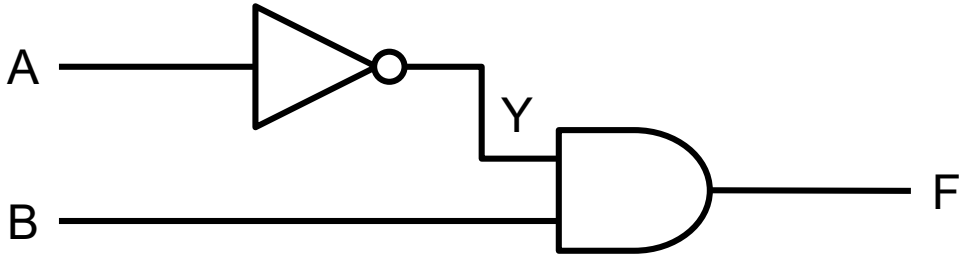
AND 게이트

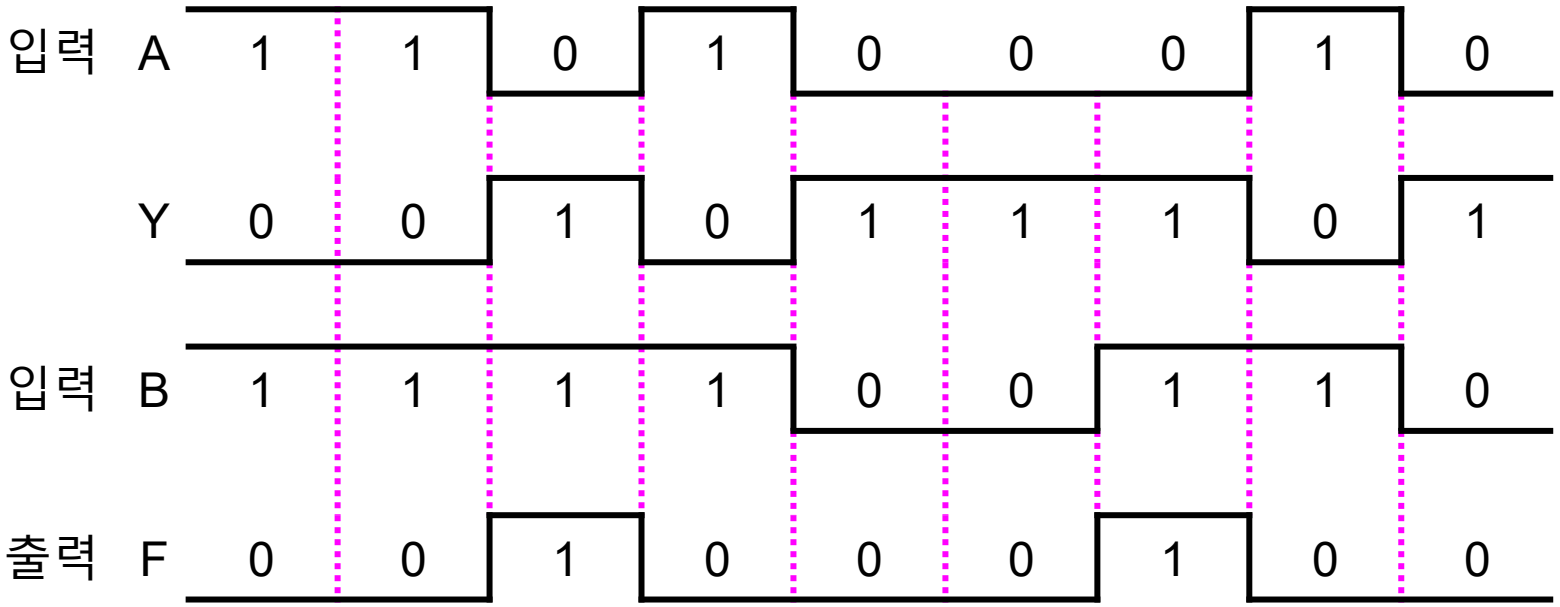
- 동작 파형


A
B
C
F


입력 A 0 0 0 0 1 1 1 1 0
입력 B 0 0 1 1 0 0 1 1 0
입력 C 0 1 0 1 0 1 0 1 0
출력 F 0 0 0 0 0 0 0 1 0

AND 게이트

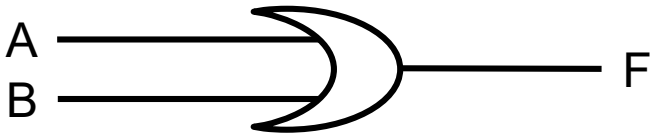

A
Y
B
F


입력 A 1 1 0 1 0 0 0 1 0
Y 0 0 1 0 1 1 1 0 1
입력 B 1 1 1 1 0 0 1 1 0
출력 F 0 0 1 0 0 0 1 0 0

OR 게이트

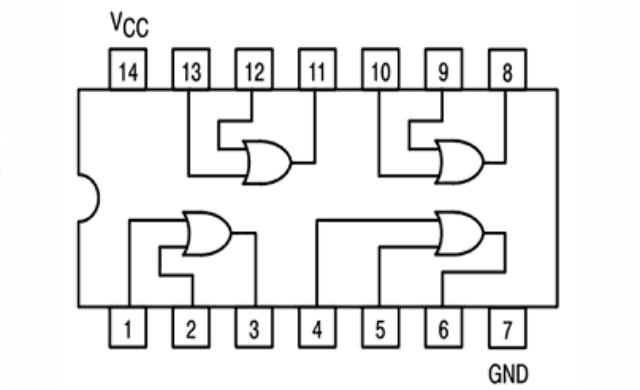
- 입력 **모두 0**인 경우에만 출력 **0** 됨
  - 입력 두 개 이상
  - 출력 한 개
  - 예, 2입력 OR 게이트의 경우 F = A + B

2입력 OR



진리표

입력		출력
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

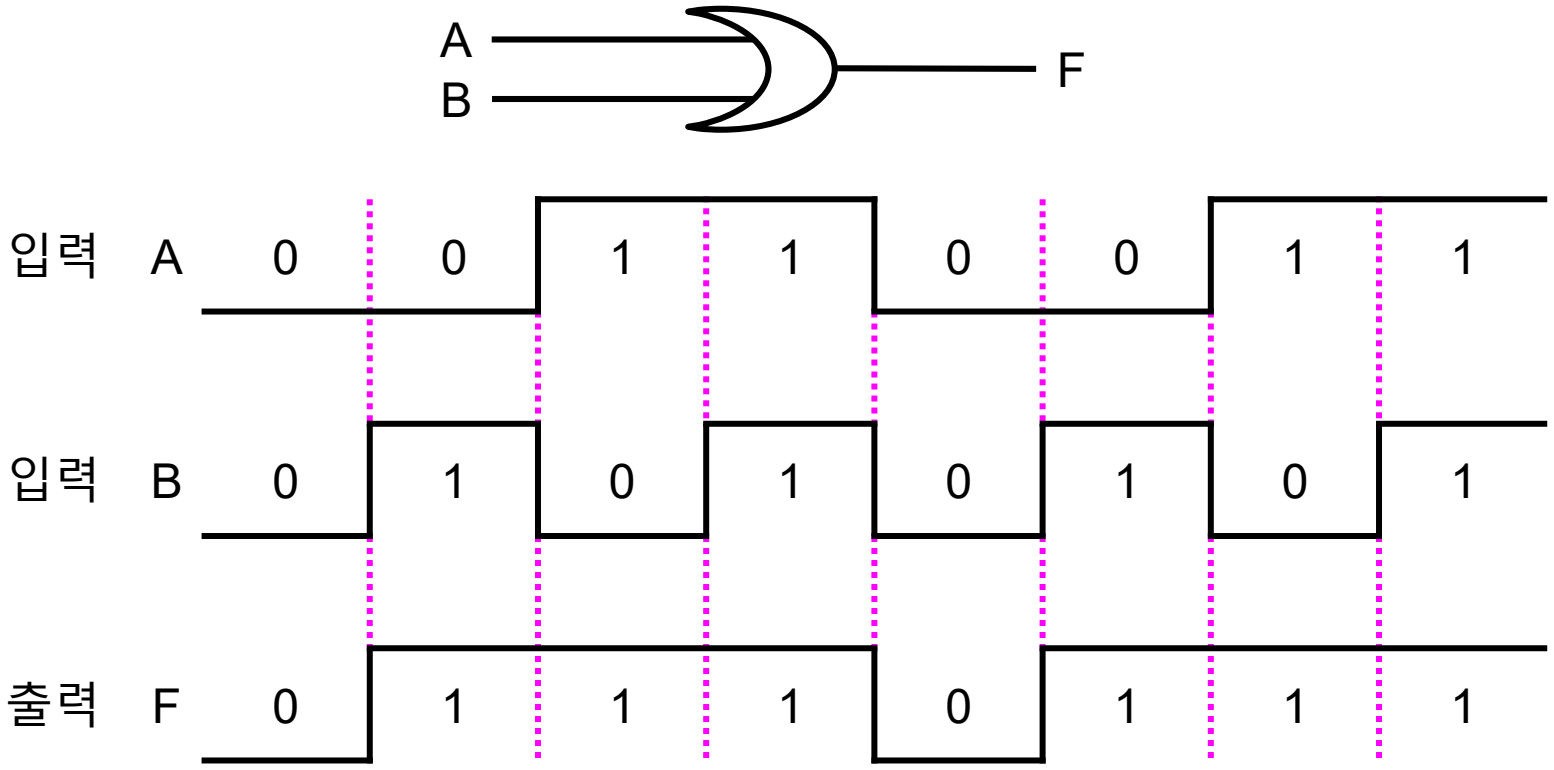


IC 7432 Quad 2-Input OR Gates

Source: STMicroelectronics, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/21733/ (accessed on 2024.08.05).

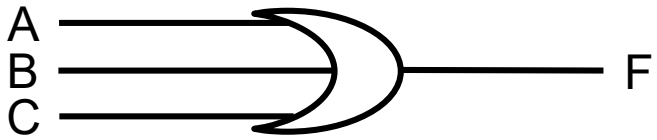
OR 게이트

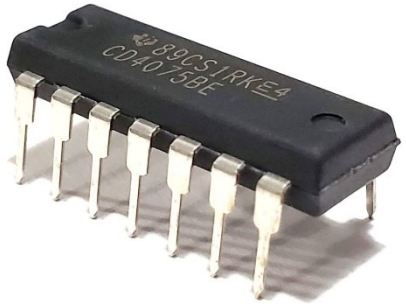
- 동작 파형

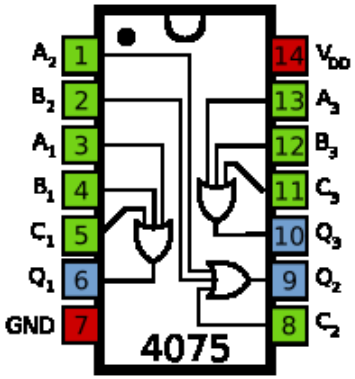


OR 게이트

- 3입력 OR 게이트
  - F = A + B + C







IC 4075 Triple 3-Input OR Gates

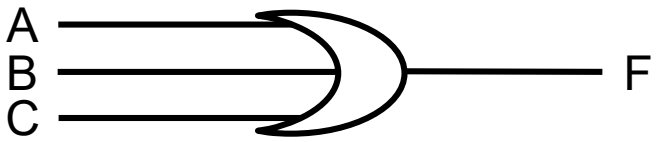
진리표

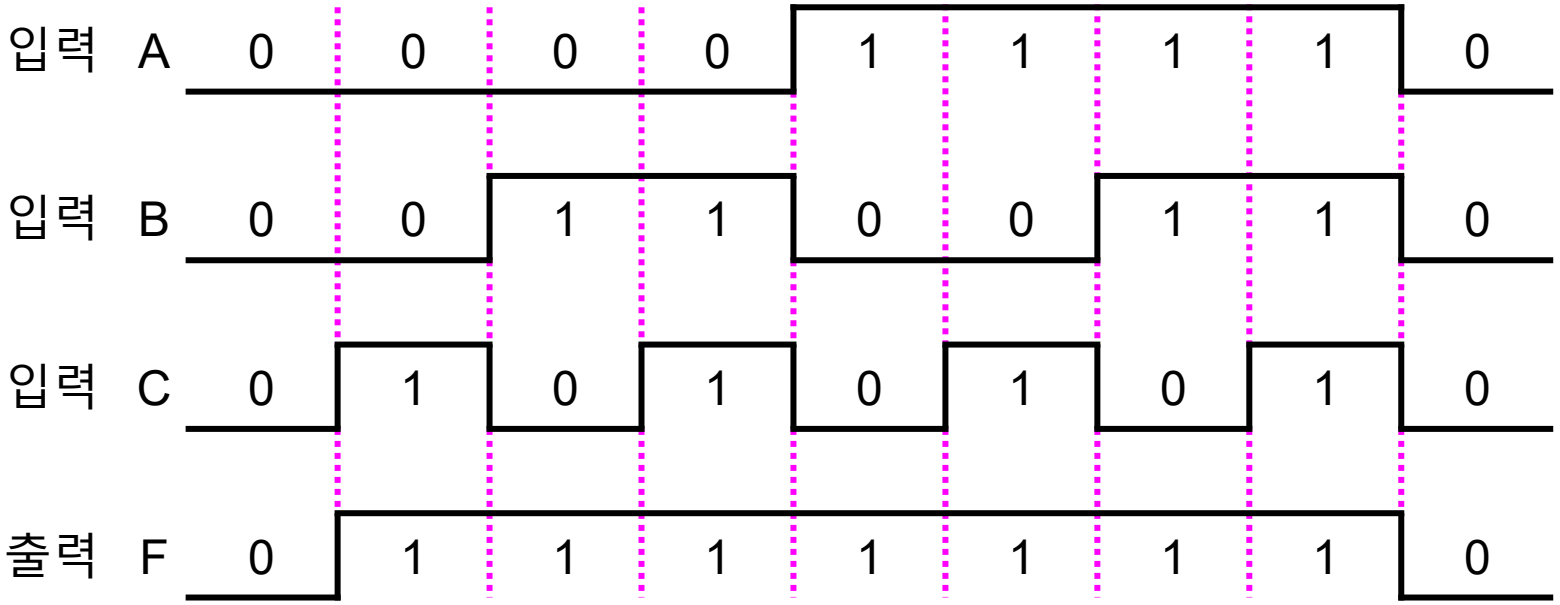
입력			출력
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Source: Texas Instruments, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/834679/ (accessed on 2024.08.05).

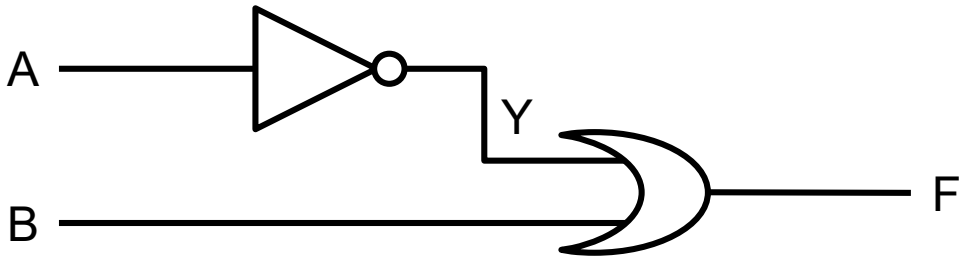
OR 게이트

- 동작 파형


A
B
C
F


입력 A 0 0 0 0 1 1 1 1 0
입력 B 0 0 1 1 0 0 1 1 0
입력 C 0 1 0 1 0 1 0 1 0
출력 F 0 1 1 1 1 1 1 1 0

OR 게이트

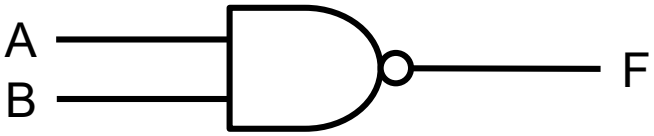


입력	A	1	1	0	1	0	0	0	1	0
	Y	0	0	1	0	0	1	1	0	1
입력	B	1	1	1	1	0	0	1	1	0
출력	F	1	1	1	1	0	1	1	1	1

NAND 게이트

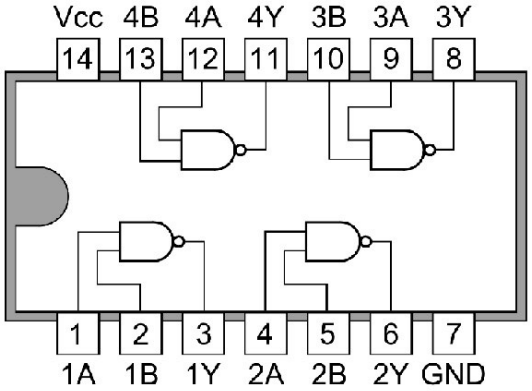
- 입력 **모두 1**인 경우에만 출력 **0** 됨
  - 입력 두 개 이상
  - 출력 한 개
  - 예, 2입력 NAND 게이트의 경우 F = $\overline{A \cdot B}$ = $\overline{AB}$

2입력 NAND



진리표

입력		출력
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

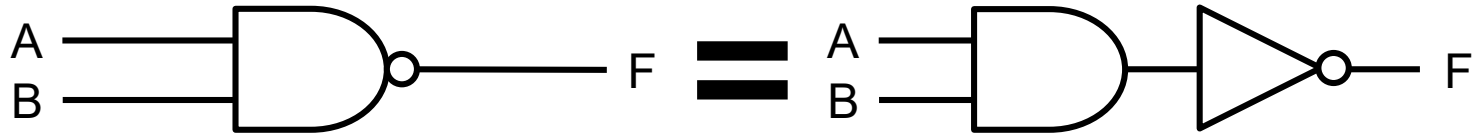


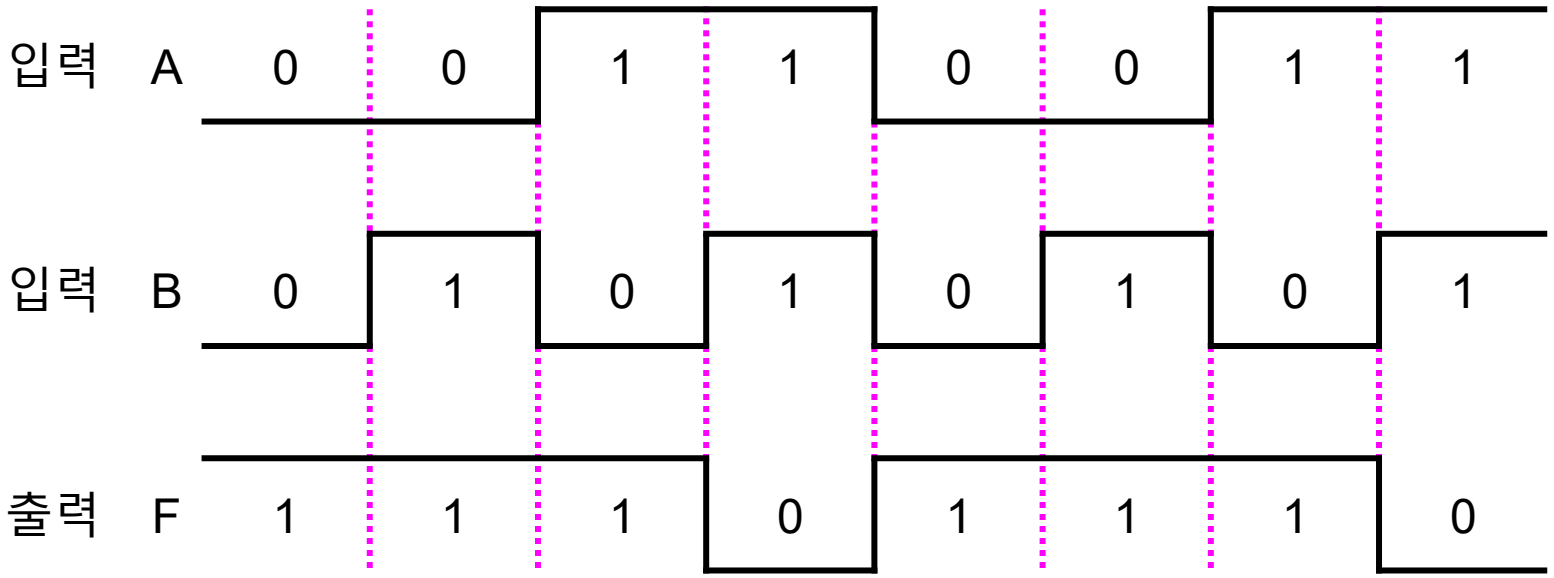
IC 7400 Quad 2-Input NAND Gates

Source: Fairchild Semiconductor, *Datasheet*, https://pdf1.alldatasheet.co.kr/datasheet-pdf/view/53738/ (accessed on 2024.08.05).

NAND 게이트

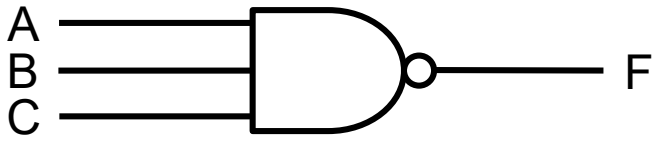
- 동작 파형

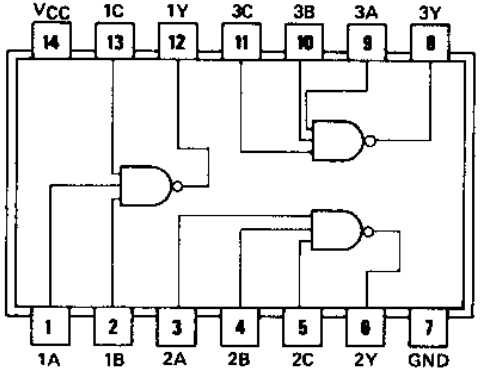




NAND 게이트

- 3입력 NAND 게이트
  - F = $\overline{ABC}$





IC 7410 Triple 3-Input NAND Gates

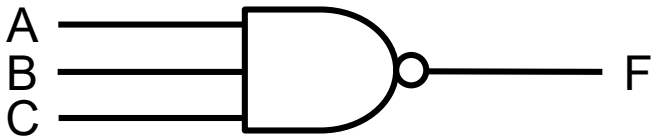
진리표

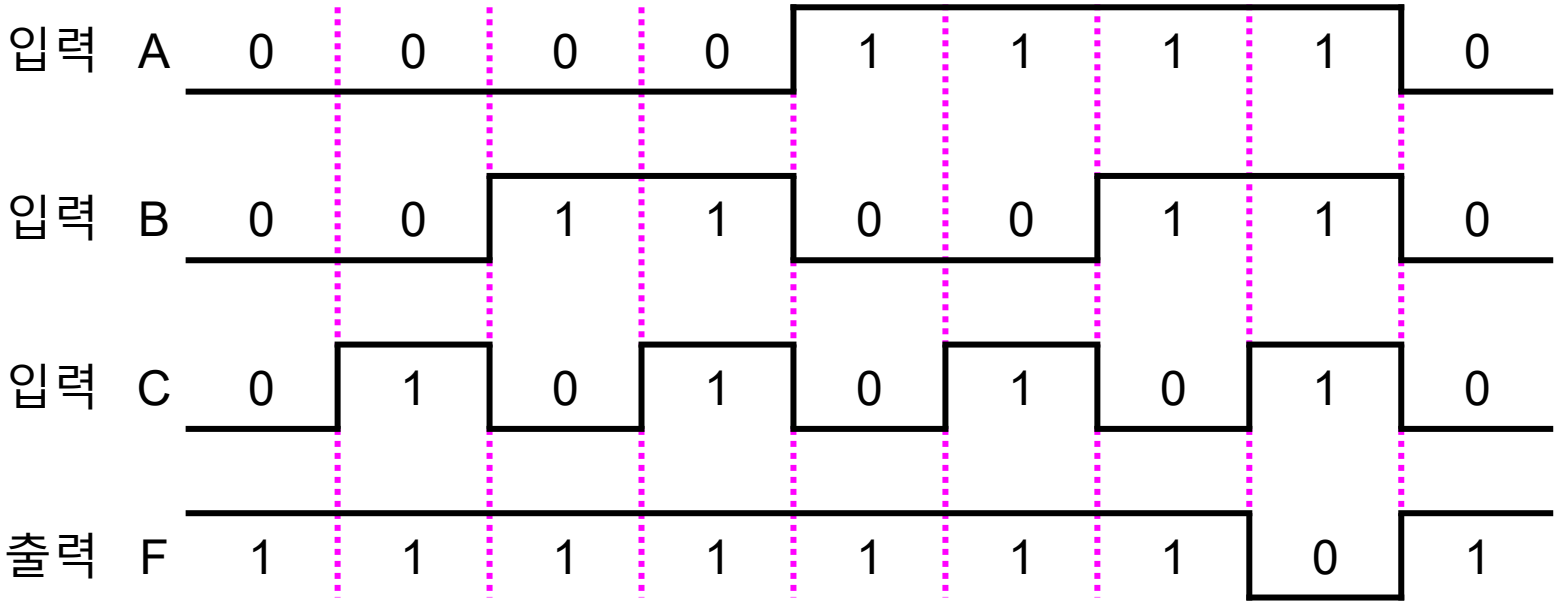
입력			출력
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Source: Texas Instruments, *Datasheet*, https://pdf1.alldatasheet.co.kr/datasheet-pdf/view/7823/ (accessed on 2024.08.05).

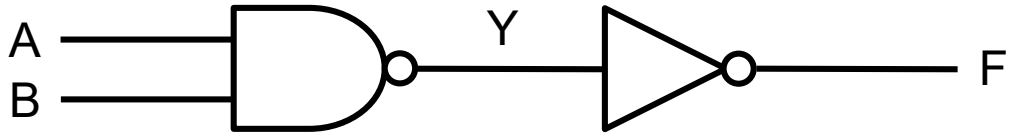
NAND 게이트

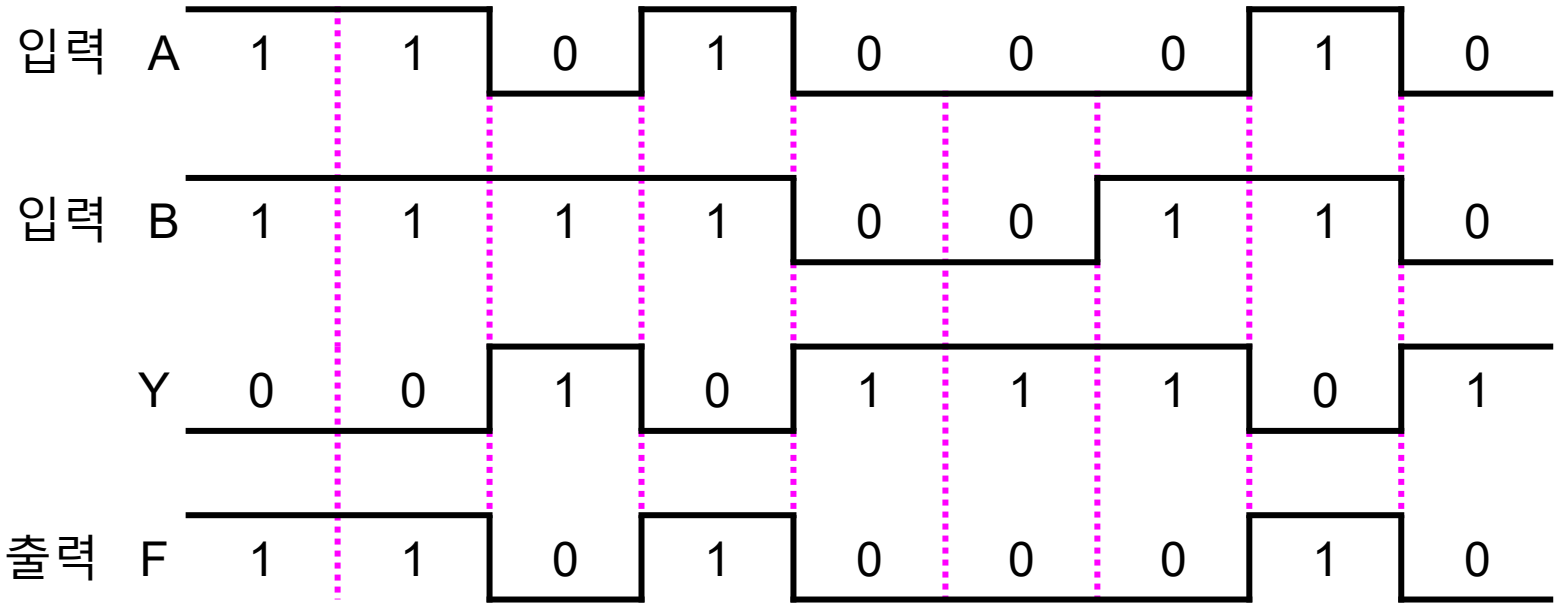
- 동작 파형





NAND 게이트

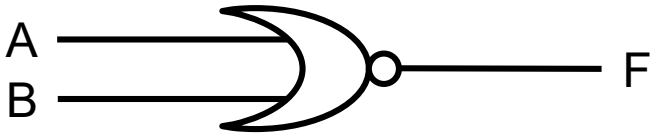

A
B
Y
F

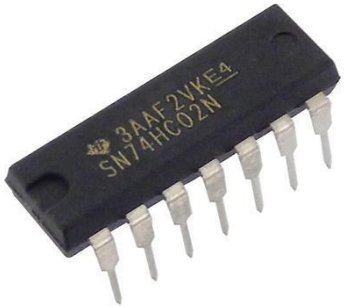

입력 A 1 1 0 1 0 0 0 1 0
입력 B 1 1 1 1 0 0 1 1 0
Y 0 0 1 0 1 1 1 0 1
출력 F 1 1 0 1 0 0 0 1 0

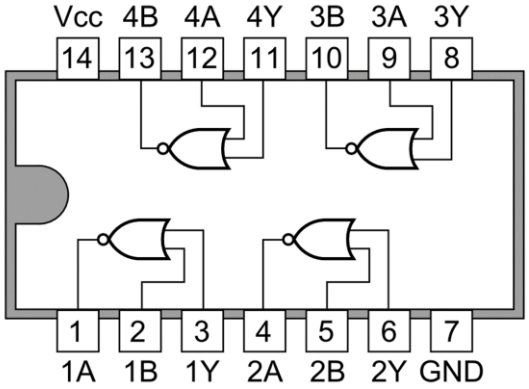
NOR 게이트

- 입력 **모두 0**인 경우에만 출력 **1** 됨
  - 입력 두 개 이상
  - 출력 한 개
  - 예, 2입력 NOR 게이트의 경우 F = $\overline{A + B}$

2입력 NOR







IC 7402 Quad 2-Input NOR Gates

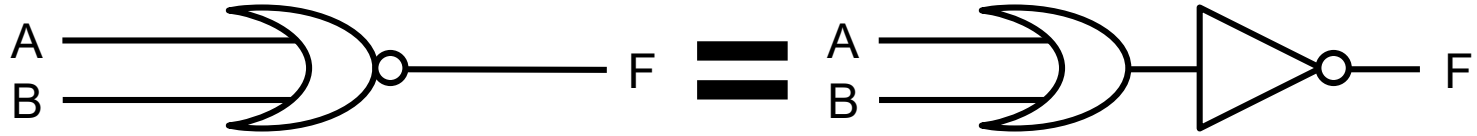
진리표

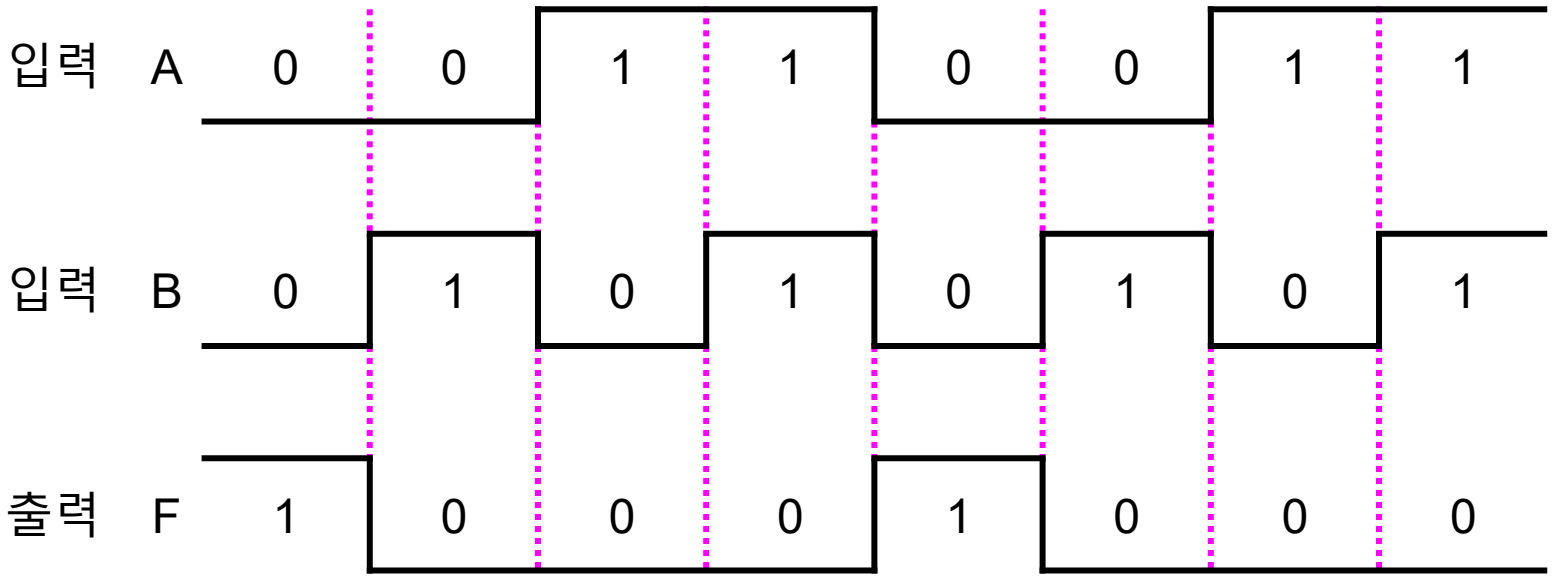
입력		출력
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Source: Fairchild Semiconductor, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/50887/ (accessed on 2024.08.05).

NOR 게이트

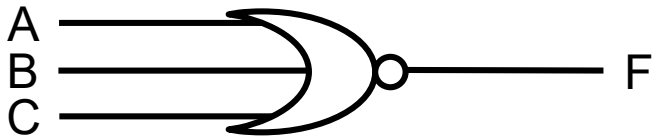
- 동작 파형

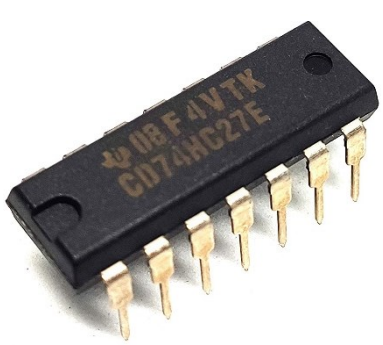


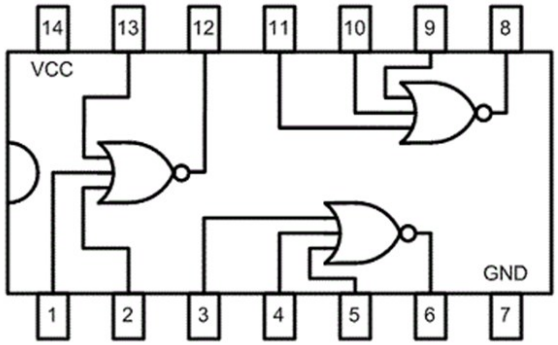


NOR 게이트

- 3입력 NOR 게이트
  - $F = \overline{A + B + C}$







IC 7427 Triple 3-Input NOR Gates

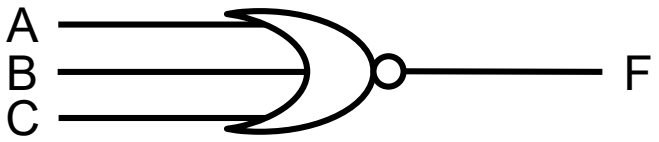
진리표

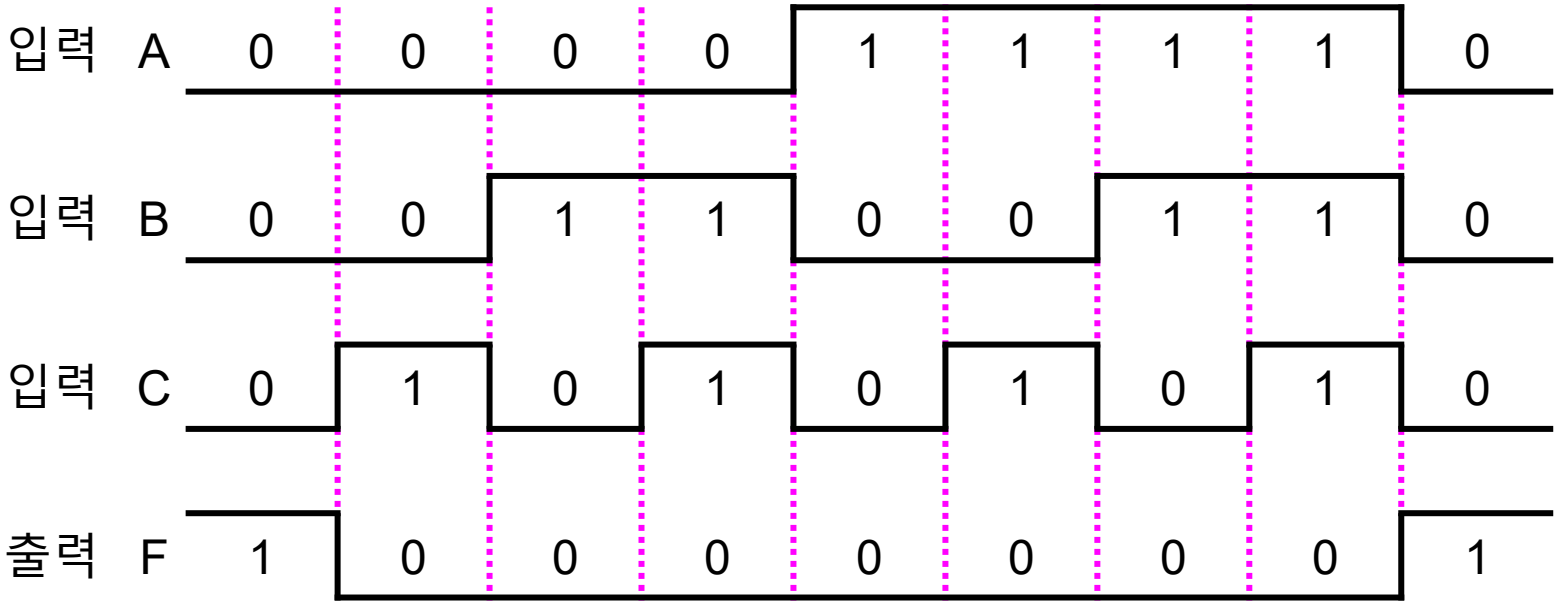
입력			출력
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Source: Fairchild Semiconductor, *Datasheet*, https://pdf1.alldatasheet.co.kr/datasheet-pdf/view/50654/ (accessed on 2024.08.05).

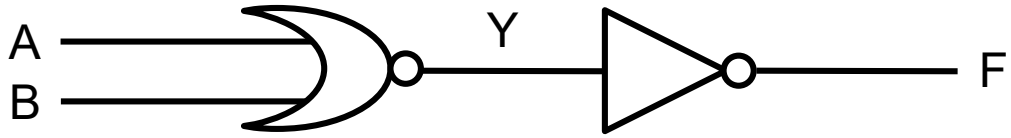
NOR 게이트

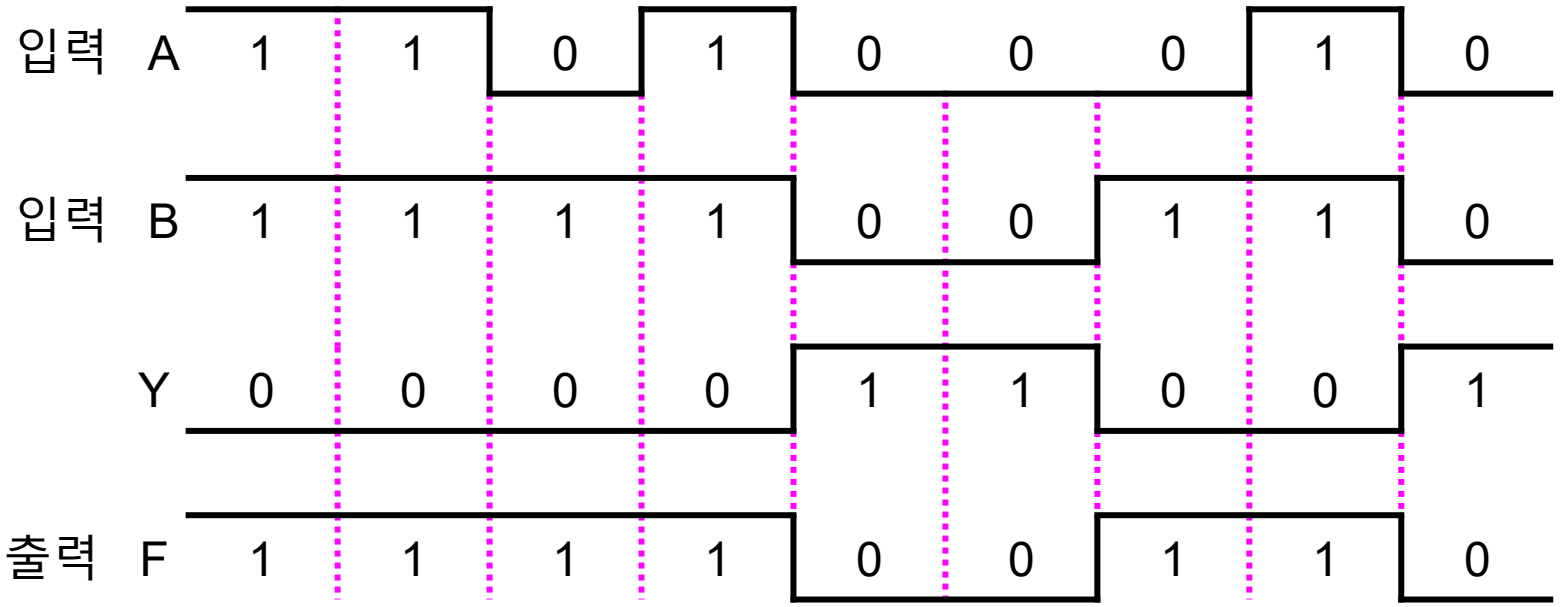
- 동작 파형


A
B
C
F


입력 A 0 0 0 0 1 1 1 1 0
입력 B 0 0 1 1 0 0 1 1 0
입력 C 0 1 0 1 0 1 0 1 0
출력 F 1 0 0 0 0 0 0 0 1

NOR 게이트


A
B
Y
F


입력 A 1 1 0 1 0 0 0 1 0
입력 B 1 1 1 1 0 0 1 1 0
Y 0 0 0 0 1 1 0 0 1
출력 F 1 1 1 1 0 0 1 1 0

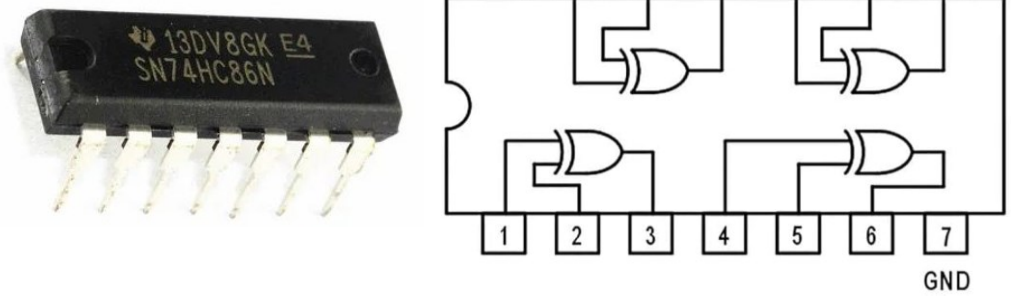
XOR 게이트

- **홀수 개의 1**이 입력된 경우에 출력 **1** 됨
  - 입력 두 개 이상
  - 출력 한 개
  - 예, 2입력 XOR 게이트의 경우 F = A ⊕ B

2입력 XOR

진리표

입력		출력
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

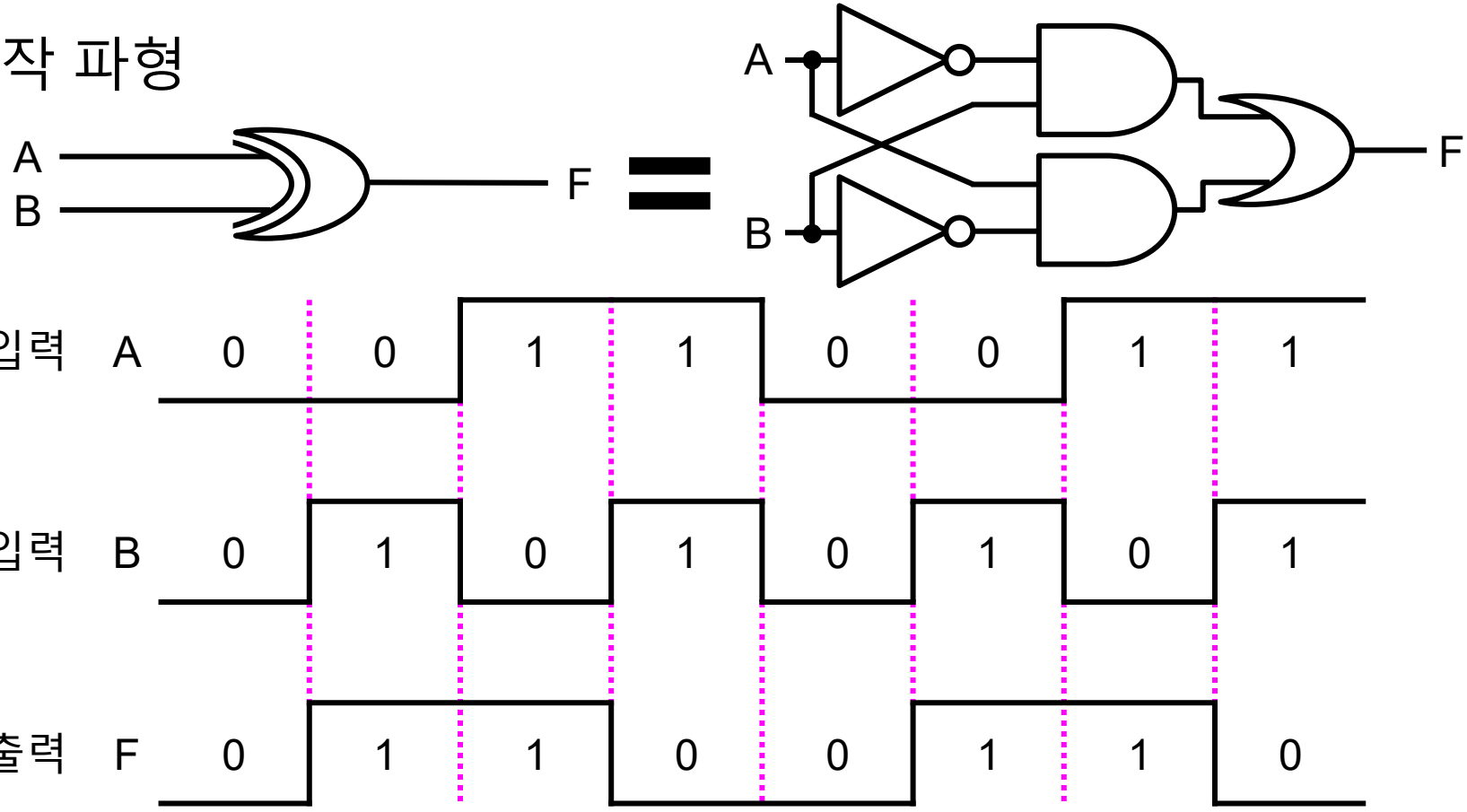


IC 7486 Quad 2-Input XOR Gates

Source: Fairchild Semiconductor, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/50914/ (accessed on 2024.08.05).

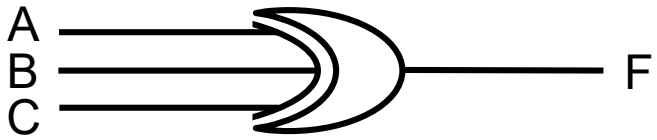
XOR 게이트

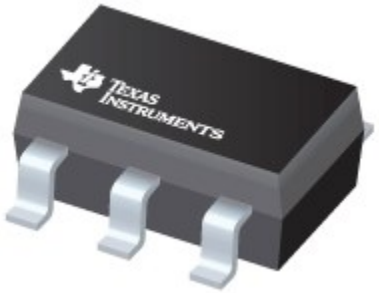
- 동작 파형

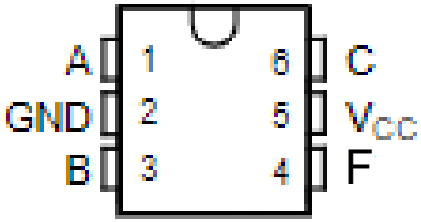


XOR 게이트

- 3입력 XOR 게이트
  - F = A ⊕ B ⊕ C







IC 74386 Single 3-Input XOR Gate

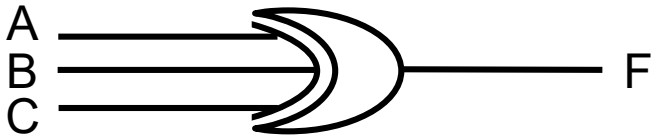
진리표

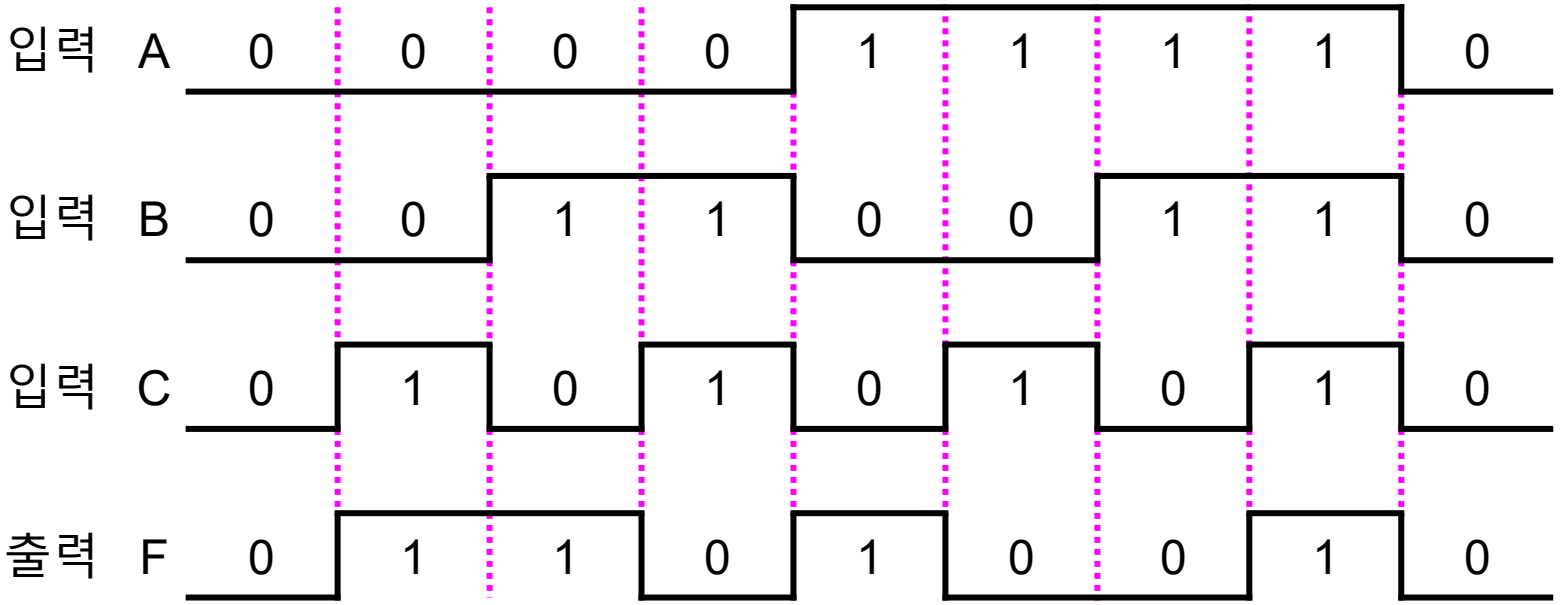
입력			출력
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Source: Texas Instruments, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/96471/ (accessed on 2024.08.05).

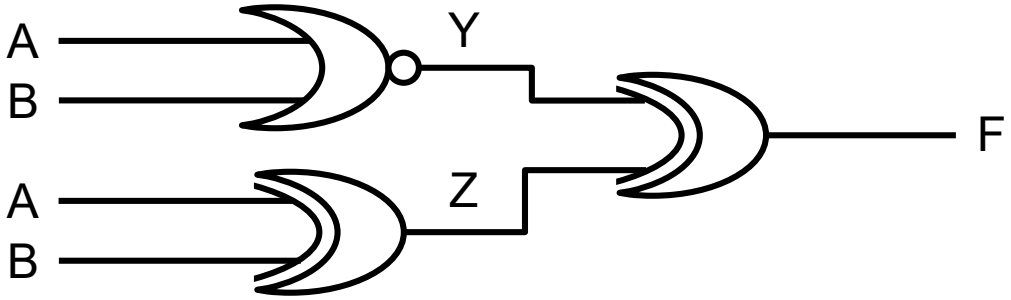
XOR 게이트

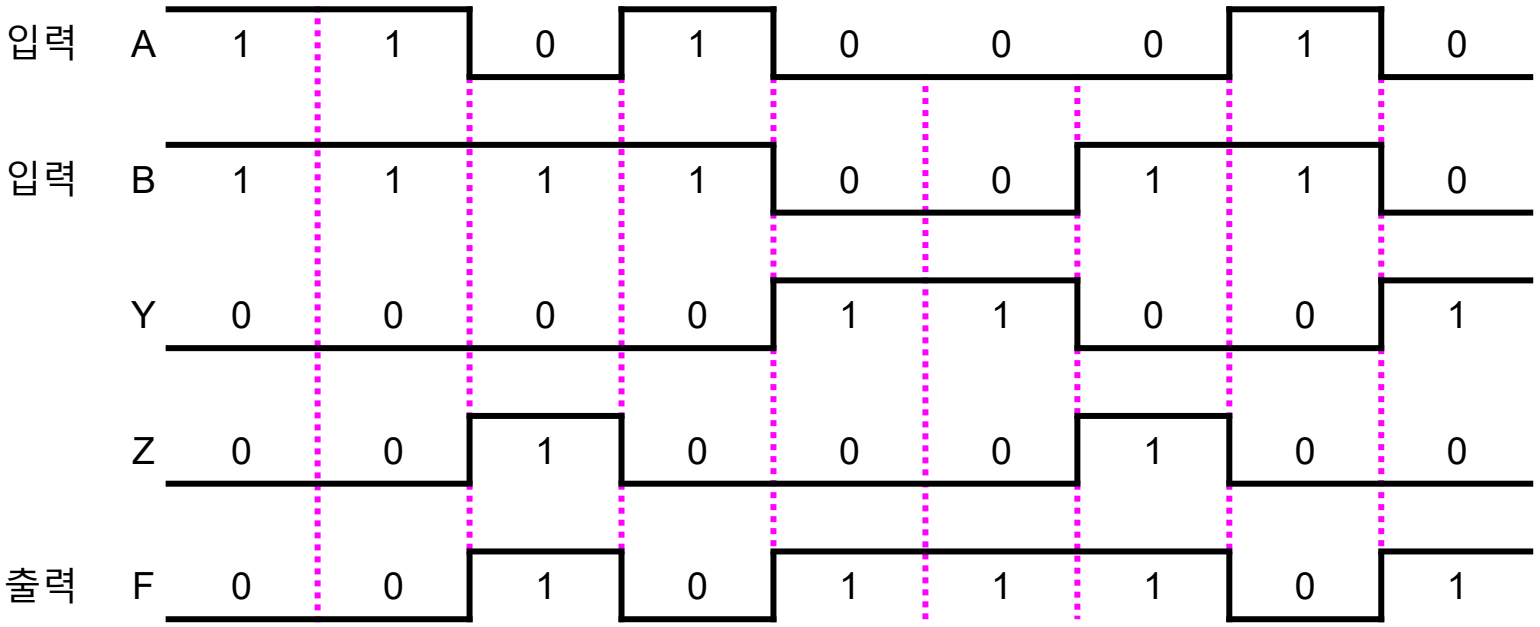
- 동작 파형


A
B
C
F


입력 A 0 0 0 0 1 1 1 1 0
입력 B 0 0 1 1 0 0 1 1 0
입력 C 0 1 0 1 0 1 0 1 0
출력 F 0 1 1 0 1 0 0 1 0

XOR 게이트

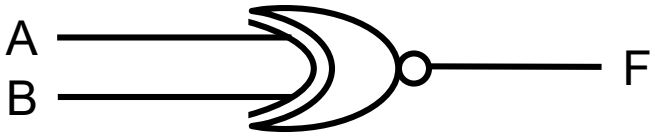

A
B
Y
A
B
Z
F

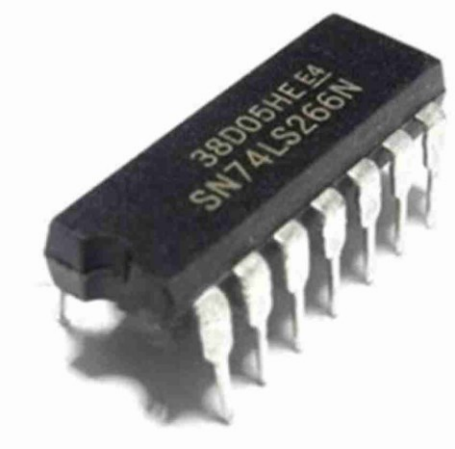

입력 A 1 1 0 1 0 0 0 1 0
입력 B 1 1 1 1 0 0 1 1 0
Y 0 0 0 0 1 1 0 0 1
Z 0 0 1 0 0 0 1 0 0
출력 F 0 0 1 0 1 1 1 0 1

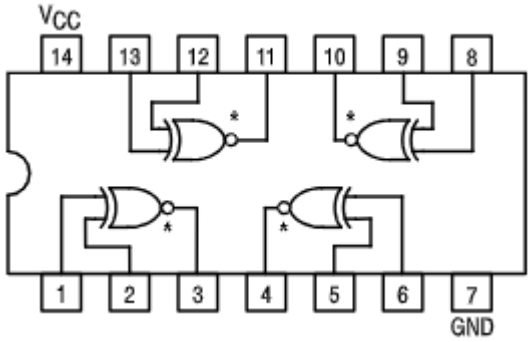
XNOR 게이트

- **짝수 개의 1**이 입력된 경우에 출력 **1** 됨
  - 입력 두 개 이상
  - 출력 한 개
  - 예, 2입력 XNOR 게이트의 경우 F = $\overline{A \oplus B}$

2입력 XNOR







IC 74266 Quad 2-Input XNOR Gates

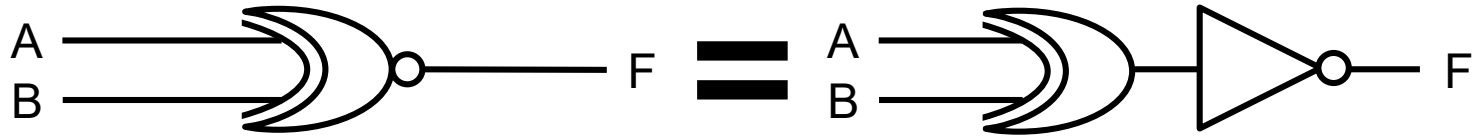
진리표

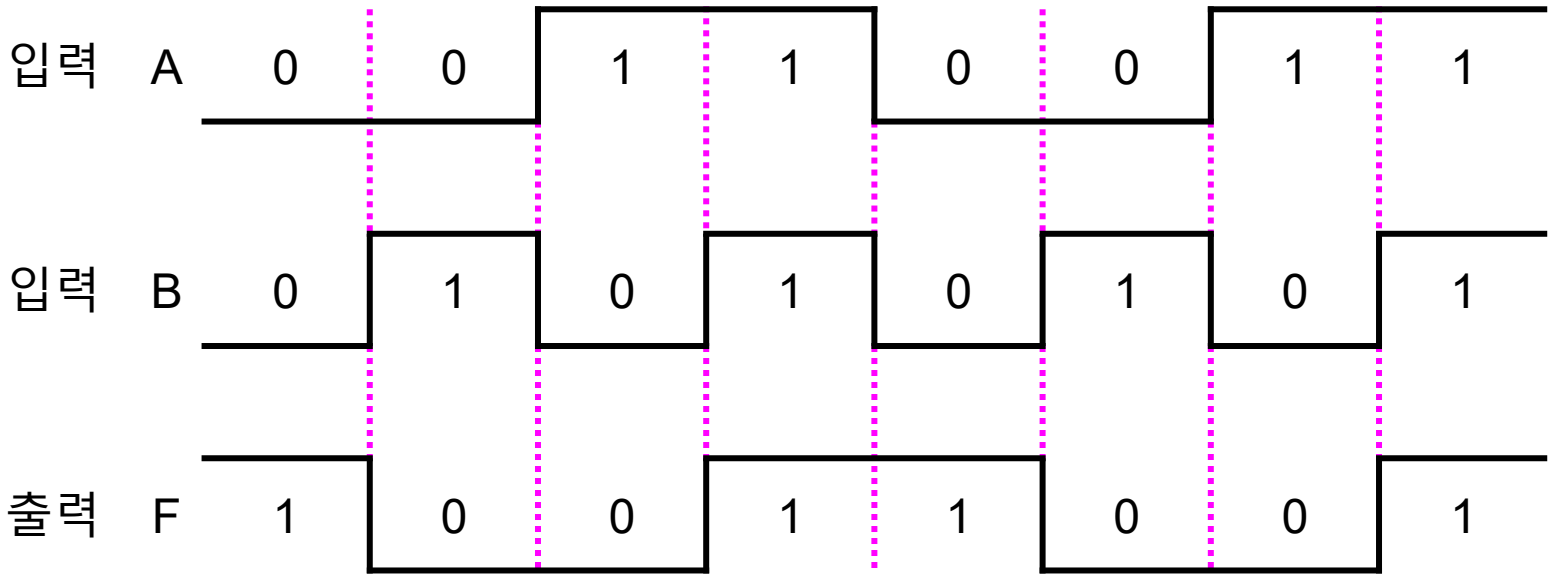
입력		출력
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

Source: Motorola, *Datasheet*, https://pdf1.alldatasheet.com/datasheet-pdf/view/5701/ (accessed on 2024.08.05).

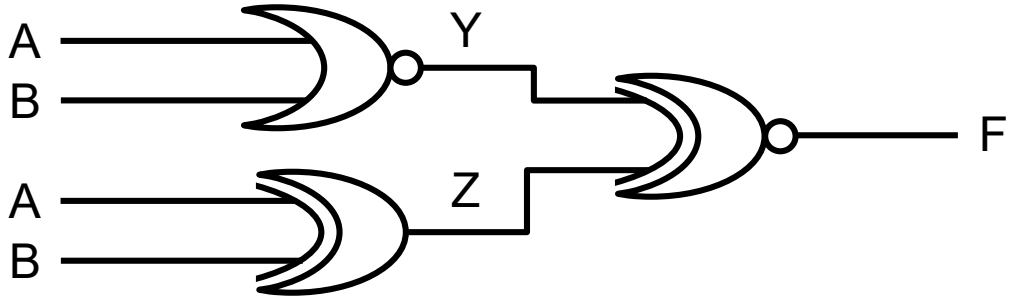
XNOR 게이트

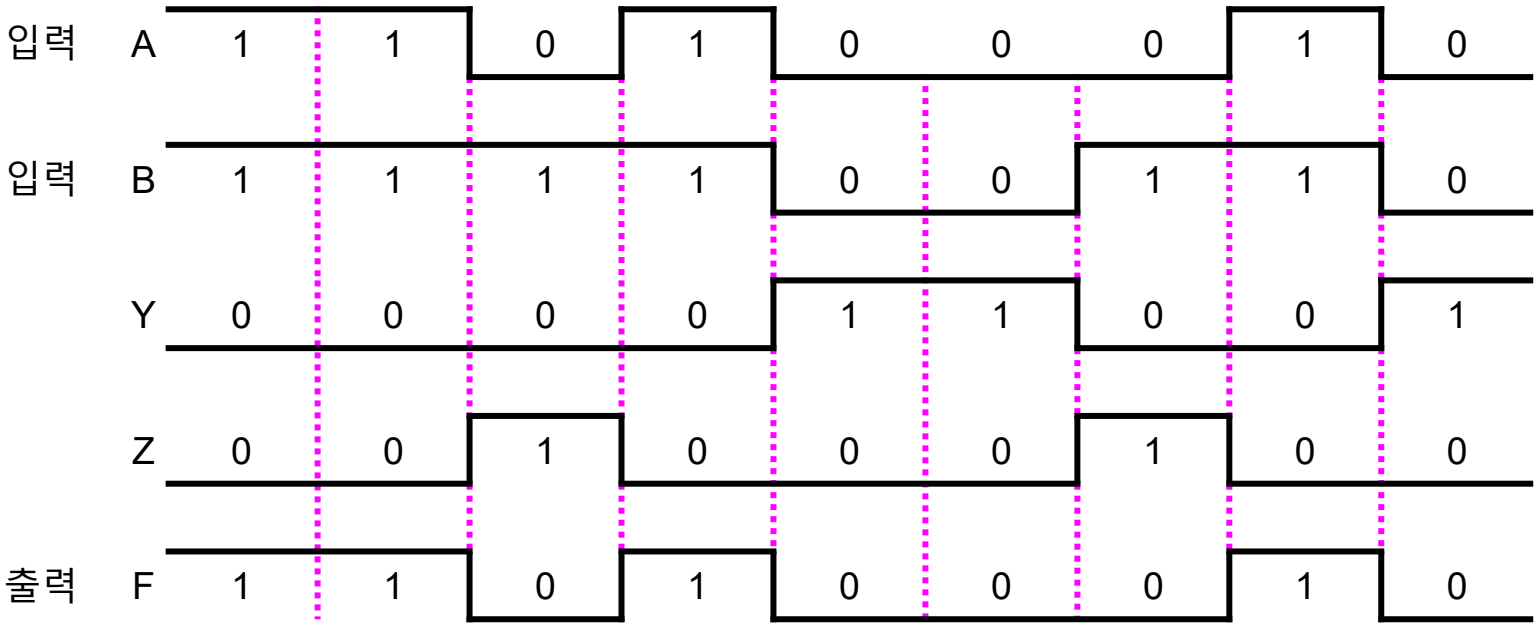
- 동작 파형





XOR 게이트

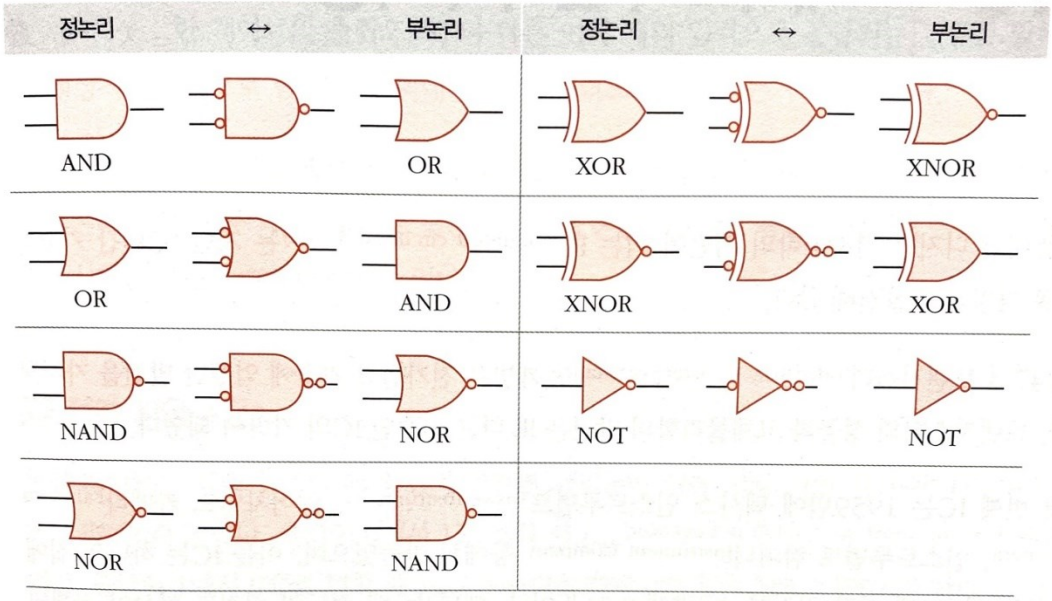

A
B
Y
A
B
Z
F


입력 A 1 1 0 1 0 0 0 1 0
입력 B 1 1 1 1 0 0 1 1 0
Y 0 0 0 0 1 1 0 0 1
Z 0 0 1 0 0 0 1 0 0
출력 F 1 1 0 1 0 0 0 1 0

정논리 및 부논리

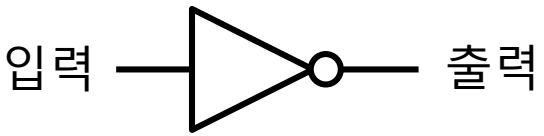
- 정논리
  - 전압 레벨 0 : Low 레벨
  - 전압 레벨 1 : High 레벨
- 부논리
  - 전압 레벨 0 : High 레벨
  - 전압 레벨 1 : Low 레벨

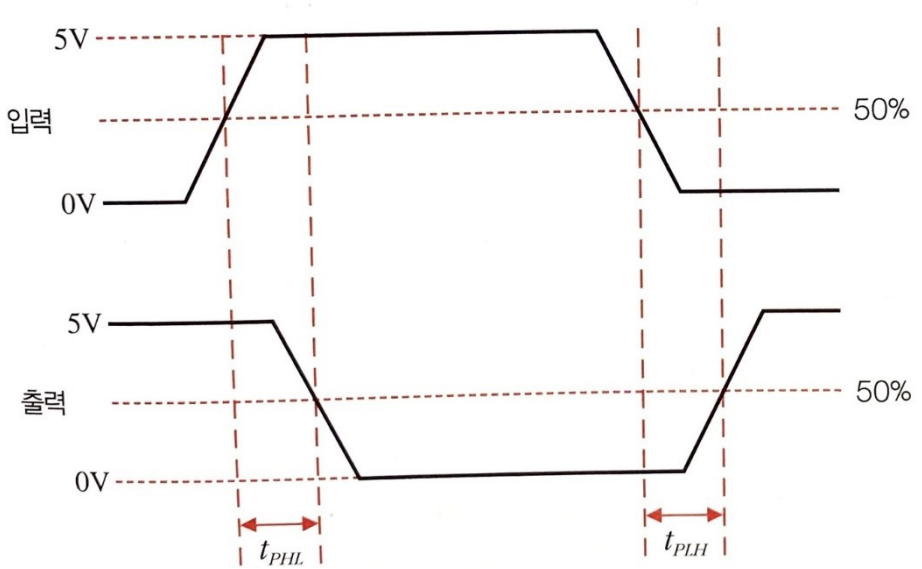
→ 표현 방법이 다를 뿐 정논리와 부논리는 **논리적으로 같음**



게이트의 전기적 특성

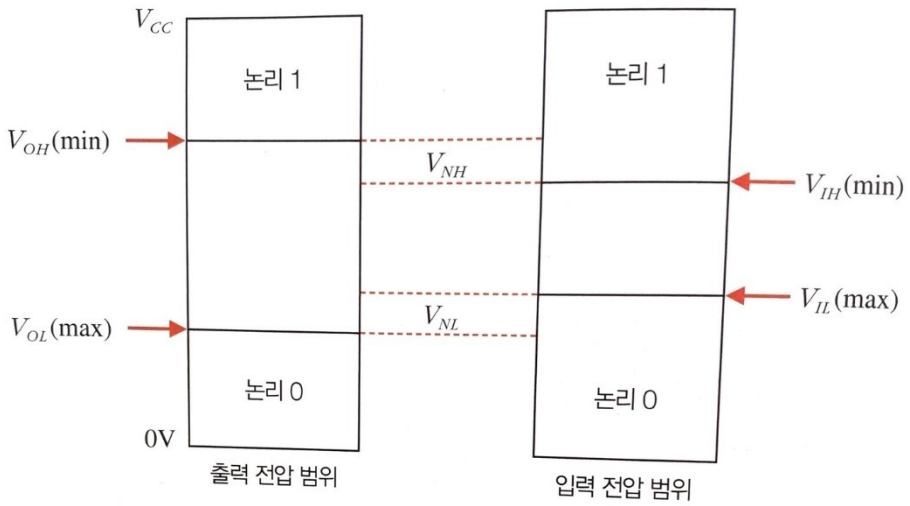
- 전파 지연 시간
  - 출력이 0에서 1로 변할 때 t_{PLH}라고 함
  - 출력이 1에서 0으로 변할 때 t_{PHL}이라고 함
  - t_{PLH}와 t_{PHL}은 입력이 50%가 될 때부터 출력이 50%가 될 때까지 측정함





게이트의 전기적 특성

- 전력 소모
  - 공급 전압과 공급 전류의 곱 : $P_{CC} = V_{CC} \times I_{CC}$ (Watts)
- 잡음 여유도
  - High 레벨의 잡음 여유도 : $V_{NH} = V_{OH}(min) - V_{IH}(min)$
  - Low 레벨의 잡음 여유도 : $V_{NL} = V_{IL}(max) - V_{OL}(max)$



게이트의 전기적 특성

- 팬-인(**fanin**) 및 팬-아웃(**fanout**)
  - Fanin : 한 개의 게이트 입력에 접속할 수 있는 최대 입력단의 수
  - Fanout : 정상적인 동작에 영향을 주지 않고, 한 게이트에서 다른 게이트로의 입력으로 연결 가능한 최대 출력단의 수
- 싱크(**sink**) 전류 및 소스(**source**) 전류
  - Sink : 출력 쪽으로 전류가 흘러 들어간다는 뜻임
  - Source : 출력에서 바깥으로 전류가 흐른다는 뜻임